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[Claim(s)]

[Claim 1] In the semiconductor device with which it comes to form the wiring pad by which said electrode terminal is connected to the substrate which array formation of two or more electrode terminals is carried out, and carries said carried member in a carried member said electrode terminal It is the semiconductor device with which it is constituted as two or more I/O cels which contain the electrode terminal for signals at least, and by which grouping was carried out for two or more electrode terminals of every, and said I/O cel is characterized by the thing of said carried member arranged at least in the location by the side of the periphery section, and the location by the side of the inner circumference section, respectively.

[Claim 2] It is the semiconductor device according to claim 1 characterized by being a package substrate for said carried member being a semiconductor chip and said electrode terminal being the internal electrode arranged on the underside of said semiconductor chip, and said substrate carrying said semiconductor chip and constituting a package.

[Claim 3] It is the semiconductor device according to claim 1 characterized by being a substrate for mounting for said carried member being the semiconductor package which carried the semiconductor chip on the package substrate, and said electrode terminal being the ball electrode for mounting arranged on the underside of said package substrate, and said substrate mounting said semiconductor package and constituting a necessary circuit.

[Claim 4] Said I/O cel is a semiconductor device according to claim 1 to 3 characterized by consisting of only electrode terminals for signals, or being constituted where each electrode terminal for the object for signals, the object for power sources, and touch-down is intermingled.

[Claim 5] The semiconductor device according to claim 4 characterized by including peripheral one in said I/O cel.

[Claim 6] Said wiring line which a wiring line is connected to said wiring pad, and is connected to each wiring pad of at least one I/O cel is a semiconductor device according to claim 1 to 5 characterized by being formed in the same wiring layer.

[Claim 7] Said substrate is a semiconductor device according to claim 6 characterized by forming the wiring line electrical connection is carried out [the line] to said wiring pad and said wiring pad by the wiring layer of one layer formed in the front face.

[Claim 8] The wiring line connected to the I/O cel arranged in the location by the side of the inner circumference section is a semiconductor device according to claim 7 characterized by carrying out extended arrangement among two or more I/O cels arranged in the location by the side of the periphery section.

[Claim 9] Said substrate is a semiconductor device according to claim 6 characterized by forming said wiring pad and the wiring line by which electrical connection is carried out to said wiring pad as a multilayer wiring layer.

[Claim 10] The semiconductor device according to claim 9 which divides said I/O cel into the 1st I/O cel by the side of the periphery section, and the 2nd I/O cel by the side of the inner circumference section, and is characterized by having arranged some I/O cels in the outside location of said carried member, and having arranged other I/O cels in the inside location at least in one side of said 1st I/O cel and 2nd I/O cel.

[Claim 11] The wiring line connected to the wiring pad corresponding to said 1st I/O cel and the wiring line connected to the wiring pad corresponding to said 2nd I/O cel are a semiconductor device according to claim 10 characterized by being formed in a wiring layer different, respectively.

[Claim 12] It is the manufacture approach of a semiconductor device of coming to form

the wiring pad by which said electrode terminal is connected to the substrate which array formation of two or more electrode terminals is carried out, and carries said carried member in a carried member. In case array formation of said electrode terminal is carried out at said carried member, said electrode terminal is constituted as two or more I/O cels which contain the electrode terminal for signals at least and by which grouping was carried out for two or more electrode terminals of every. The manufacture approach of the semiconductor device characterized by arranging said a part of I/O cel in the location by the side of the periphery section of said carried member, and arranging other I/O cels rather than said some of I/O cels in the location by the side of the inner circumference section of said carried member.

[Claim 13] The manufacture approach of the semiconductor device according to claim 12 characterized by arranging the I/O cel concerned which cannot be arranged in the location by the side of the inner circumference section of said carried member when the I/O cel which cannot be arranged when said a part of I/O cel has been arranged in the location by the side of the periphery section of said carried member arises.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which aimed at cutback-izing of a chip or a package, and buildup of the number of terminals of an external electrode terminal especially about the area array semiconductor device which arranged the external electrode terminal on the chip underside or the package underside, and its manufacture approach.
[0002]
[Description of the Prior Art] It is in the inclination for the number of terminals of the external electrode terminal for carrying out electrical connection of the package carrying the internal electrode terminal for carrying out electrical connection of the chip outside or a chip outside with high integration of a semiconductor device to increase. Moreover, on the other hand, the miniaturization of a chip or a package is advanced, and the pitch between terminals of an internal electrode terminal is micrified. Therefore, the array pitch of the wiring pad formed in the mounting substrate for mounting the array pitch of the wiring pad formed in the package substrate at the time of carrying the chip concerned in a package substrate and constituting a package or a package will also be micrified, the case where leading about of wiring in these package substrate or a mounting substrate becomes impossible is, and realizing has become with a difficult thing about the miniaturization of a chip or a package as the result.
[0003] For example, drawing 11 is the example of the semiconductor device 101 which formed the internal electrode terminal in the underside of a chip, carried the chip in the package substrate, and constituted the package. As for the chip 103, the ball electrode 131 as many external electrode terminals is formed in the underside in the BGA (Ball Grid Array) array. Moreover, the package substrate 102 is taking about the wiring line 122 linked to each wiring pad 121 while the wiring pad 121 corresponding to the ball electrode 131 of said chip 103 is arranged on the front face. Moreover, array formation of the ball electrode 124 for mounting connected to the rear face of said package substrate 102 through through hole 123 grade on said wiring pad 121 and wiring line 122 is carried out. And it is carried on said package substrate 102, and the ball electrode 131 is connected by soldering etc. to the wiring pad 121, and coat closure of said chip 103 is carried out with resin 105. Moreover, said semiconductor device 101 is mounted on the substrate 104 for mounting, said ball electrode 124 for mounting is connecting with the wiring pad 141 formed in the top face of the substrate 104 for mounting, and the mounting is performed.
[0004] Drawing 12 is drawing showing typically the array condition of the wiring pad 121 arranged on the front face of said package substrate 102. In addition, the array condition of this wiring pad 121 serves as an array of said ball electrode 131 formed in the underside of a chip 103 as it was. In the array of the conventional wiring pad, it has the composition of having arranged what has arranged the signal-line terminal (switch terminal) called peripheral [so-called], the power supply terminal (V terminal), and the earth terminal (G terminal) in a straight line to the field corresponding to the periphery section of a chip 103. Each wiring pad 121 of a switch terminal, V terminal, and G terminal is arranged in the shape of a grid at the necessary spacing so that the amplification graphic display of the part may be carried out in this drawing. And although the wiring line 122 is connected to each wiring pad 121 and pulled out towards the outside field of a chip The wiring line 122 linked to the

wiring pad 121 arranged inside The drawer is performed through between the wiring pads 121 arranged outside, and as the pulled-out point was shown in drawing 9 , the through hole 123 grade is performing electrical connection to the Boru electrode 124 for mounting of the underside of the package substrate 102.

[0005] However, with such array structure of a wiring pad, as the array consistency of the wiring pad 121 and the wiring line 122 is shown in drawing 13 , since the diameter size method of the wiring pad 121 is larger than the width method and line spacing of the wiring line 122, in case the wiring line 122 is pulled out from the inside wiring pad 121, generally constraint will be received in the number of the wiring line to pull out. That is, in this drawing, when are arranged in the pitch whose wiring pad 121 with a diameter of 100 micrometers is 250 micrometers, and line width of face of the wiring line 122 is set to 30 micrometers and line spacing is set to 30 micrometers, only two wiring lines 122 can be pulled out between both the wiring pads 121. That is, in the case of the array structure of this wiring pad 121, only 12 wiring lines 122 can be arranged in the dimension of 1mm, and the array consistency of a wiring line becomes in 12 [// mm and]. Therefore, if the number of wiring pads increases and the number of drawers of a wiring line increases, the area which described the pitch of a wiring pad above to make it larger than 250 micrometers, or enlarge a chip size, and for this arrange a wiring pad will increase, and it will become difficult to realize the miniaturization of a chip and a package substrate.

[0006] The wiring pad the object for reference supplies which does not deliver a signal to JP,10-116859,A with the technique of a publication, and for reference current is arranged inside a package (chip) to such a problem, and the configuration which connects the wiring pad concerned to the external connection terminal which is directly under a chip is taken. According to this configuration, since the wiring pad which does not deliver a signal does not need to connect a wiring line, it does not need to take about a wiring line for between the wiring pads arranged on that outside, can reduce spacing of an outside wiring pad, and will increase the number of wiring pads as a result, and the miniaturization of a chip can realize it.

[0007] In order to realize arrangement which, on the other hand, used effectively the free area generated between internal-circuitry blocks, without spoiling the fundamental algorithm of an automatic-layout wiring tool for JP,9-69568,A when having arranged the pad, close and an output buffer, and the internal-circuitry block for the chip, the technique which made it possible to arrange close and an output buffer to the free area which generates distinction of close and output-buffer arrangement area, and internal-circuitry block location area also in a stop and internal-circuitry block location area is indicated. If this invention applies this technique to the target package so that chip, concerning arrangement of a wiring pad at least, the degree of freedom of arrangement improves, and when attaining a miniaturization, it will become effective.

[0008]

[Problem(s) to be Solved by the Invention] However, since the former technique (JP,10-116859,A) is premised on only a certain amount of number existing by the wiring pad which does not deliver a signal, there are few this kind of wiring pads, and when it is required that a wiring line should be connected to almost all the wiring pad, it cannot apply. Moreover, even if it applies about some wiring pads, about the wiring pad to which a wiring line is connected, the problem of receiving a limit in the drawer number of a wiring line as described above is unsolvable.

[0009] since [moreover,] the latter technique (JP,9-69568,A) is not [that the number of close and the output buffers arrange is influence by the magnitude of the free area

generate between internal-circuitry blocks, or] clear in whether the drawer of the wiring line from inside close and output buffer is possible when the part which a free area generates concentrates -- every floor plan -- the design of a wiring pad -- not carry out -- it does not obtain but the processing time (TAT) becomes long. Moreover, when it becomes clear for the drawer of a wiring line to be difficult, the effective means against this does not exist and has not solved the above mentioned problem.

[0010] In addition, the above mentioned technique is carrying out the premise of the number of the wiring lines formed in a package substrate being one, and if the wiring line of a package substrate is formed in the multilayer-interconnection structure more than two-layer, it can become one technique at the time of the degree of freedom of leading about of a wiring line becoming high, and solving the above mentioned problem. However, if a wiring line is made into multilayer-interconnection structure, the situation that the wiring line connected to the same close and output circuit crosses mutually in a vertical layer may arise, and it will be hard coming to take impedance matching between each wiring line in such a case, and will have big effect on the property of a semiconductor device, and cannot be said to be a desirable thing.

[0011] While the object of this invention solves the above problem and attains the miniaturization of a chip or a package, it offers the semiconductor device which enabled buildup of the number of terminals of an external connection terminal, and its manufacture approach.

[0012]

[Means for Solving the Problem] In the semiconductor device with which, as for this invention, it comes to form the wiring pad by which said electrode terminal is connected to the substrate with which array formation is carried out and two or more electrode terminals carry said carried member in a carried member Said electrode terminal is constituted as two or more I/O cels which contain the electrode terminal for signals at least and by which grouping was carried out for two or more electrode terminals of every, and said I/O cel is characterized by the thing of said carried member arranged at least in the location by the side of the periphery section, and the location by the side of the inner circumference section, respectively. For example, said carried member is a semiconductor chip, said electrode terminal is the internal electrode arranged on the underside of said semiconductor chip, and said substrate is constituted as a package substrate for carrying said semiconductor chip and constituting a package. Or said carried member is the semiconductor package which carried the semiconductor chip on the package substrate, said electrode terminal is the ball electrode for mounting arranged on the underside of said package substrate, and said substrate is constituted as a substrate for mounting for mounting said semiconductor package and constituting a necessary circuit.

[0013] Here, said I/O cel consists of only electrode terminals for signals, or the object for signals, the object for power sources, and where each electrode terminal for touch-down is intermingled, it is constituted. Moreover, peripheral one may also be included in said I/O cel.

[0014] While according to this invention dividing electrode terminals, such as an internal electrode, into an I/O cel and arranging some of the I/O cels in the location by the side of the periphery section of carried members, such as a chip [when a chip is miniaturized by arranging other I/O cels in the location by the side of the inner circumference section rather than it] Or when the number of internal electrodes is increased, the drawer of the wiring line from the wiring pad corresponding to each I/O cel to the circumference outside of a chip becomes possible, and the semiconductor device corresponding to high integration of a semiconductor device and

high-performance-izing can be realized.

[0015] Said wiring line which a wiring line is connected to said wiring pad, and is connected to each wiring pad of at least one I/O cel in a substrate on the other hand is formed in the same wiring layer. That is, the wiring line electrical connection is carried out [a line] to said wiring pad and said wiring pad by the wiring layer of one layer by which said substrate was formed in the front face is formed. In this case, extended arrangement of the wiring line connected to the I/O cel arranged in the location by the side of the inner circumference section is carried out among two or more I/O cels arranged in the location by the side of the periphery section. Or said substrate is formed as a wiring layer of a multilayer [line / by which electrical connection is carried out to said wiring pad / said wiring pad and / wiring]. In this case, said I/O cel is divided into the 1st I/O cel by the side of the periphery section, and the 2nd I/O cel by the side of the inner circumference section, and it considers as the configuration which has arranged some I/O cels in the outside location of said carried member, and has arranged other I/O cels in the inside location at least in one side of said 1st I/O cel and 2nd I/O cel. And the wiring line connected to the wiring pad corresponding to said 1st I/O cel and the wiring line connected to the wiring pad corresponding to said 2nd I/O cel are considered as the configuration formed in a wiring layer different, respectively.

[0016] According to this invention, since the wiring pad and wiring line corresponding to an I/O cel are formed by the electric conduction film of one layer formed in the substrate, it becomes possible for the wiring line especially connected to the same I/O cel not to cross up and down, and to perform impedance matching in each wiring line easily. When two or more wiring pads and wiring lines corresponding to close and an output buffer are especially intermingled in one I/O cel, the mutual intervention between the wiring lines of each close and output buffer is prevented, and proper impedance matching becomes possible. Moreover, since it consists of wiring layers from which each wiring line corresponding to the 1st I/O cel and the 2nd I/O cel differs, even when both the I/O cel has been arranged to the periphery section [of a chip], and inner circumference section side, respectively, it becomes possible to arrange each I/O cel in an inside location and an outside location, respectively, and impedance matching in the wiring line corresponding to each I/O cel also becomes easy.

[0017] Moreover, array formation of the electrode terminal of plurality [approach / of the semiconductor device of this invention / manufacture / member / carried] is carried out. It is the manufacture approach of a semiconductor device of coming to form the wiring pad by which said electrode terminal is connected to the substrate in which said carried member is carried. In case array formation of said electrode terminal is carried out at said carried member, said electrode terminal is constituted as two or more I/O cels which contain the electrode terminal for signals at least and by which grouping was carried out for two or more electrode terminals of every. It is characterized by arranging said a part of I/O cel in the location by the side of the periphery section of said carried member, and arranging other I/O cels rather than said some of I/O cels in the location by the side of the inner circumference section of said carried member. In this case, when the I/O cel which cannot be arranged when said a part of I/O cel has been arranged in the location by the side of the periphery section of said carried member arises, the I/O cel concerned which cannot be arranged is arranged in the location by the side of the inner circumference section of said carried member. Thereby, manufacture of the semiconductor device of this invention is attained.

[0018]

[Embodiment of the Invention] Next, the operation gestalt of this invention is

collectively [the cel], and constitutes the group of this lot as one I/O cel CELL. Or the I/O cel CELL of a lot consists of only switch terminals. In addition, it is also possible for neither the number of each terminals nor its array to be restricted to the above mentioned configuration, but to constitute as an I/O cel of the array of arbitration.

[0022] Although a part of I/O cel CELL-A is arranged like before corresponding to the periphery of a chip 3 to two or more I/O cels CELL by which the group division was moreover carried out, rather than said I/O cel CELL-A, other I/O cel CELL-B sets necessary spacing, and is arranged corresponding to the inner circumference section of a chip. In this case, I/O cel CELL-A arranged at the periphery section is formed so that the necessary spacing SPACE may be secured between two I/O cel CELL-A which adjoins a hoop direction. In addition, in this operation gestalt, it arranges in the condition of having made conventional peripheral one PL intermingled, in I/O cel CELL-A of the periphery section in the part which has allowances in an adjoining field. That is, in drawing 2 , the part where the wiring pad 21 is not the array of 4x3 is the field which made peripheral one PL intermingled.

[0023] Drawing 3 is some enlarged drawings of the wiring line 22 connected to the wiring pad 21 formed in the top face of said package substrate 2, and these wiring pad 21. Here, the condition of I/O cel CELL-A of the two periphery sections arranged corresponding to the periphery section of a chip 3 having set necessary spacing, having been arranged along a hoop direction, and having been arranged in the location where I/O cel CELL-B of the one inner circumference section counters the spacing SPACE between said two I/O cel CELL-A is shown. And wiring line 22a is connected to each wiring pad 21a of two I/O cel CELL-A of the periphery section like before, respectively, and it is pulled out to the field corresponding to the circumference outside of a chip 3 through between each wiring pad 21a. Although wiring line 22b connected to each wiring pad 21b of I/O cel CELL-B arranged at the inner circumference section on the other hand is pulled out like before in the field of I/O cel CELL-B In the field from which it separated outside from the field of the I/O cel CELL-B concerned, each wiring line 22b is bundled at the necessary spacing, and is pulled out by even the circumference outside field through spacing of I/O cel CELL-A of said periphery section in this condition of having been bundled.

[0024] Therefore, with the array structure of the wiring pad 21 and the wiring line 22 in such a package substrate 2, although the array consistency of wiring line 21a in I/O cel CELL-A arranged corresponding to the periphery section of a chip 3 is conventionally [which was shown in drawing 13 R> 3] the same as a configuration As for the array consistency of wiring line 22b connected to wiring pad 21b of I/O cel CELL-B arranged corresponding to the inner circumference section of a chip 3, it becomes possible the part in which the wiring pad does not exist, and to carry out densification. That is, as shown in drawing 3 , when line width of face of the wiring line 22 connected to a total of 12 wiring pads 21 is set to 30 micrometers and line spacing is set to 30 micrometers, the dimension for bundling and arranging 12 wiring line 22i is set to 750 micrometers. If the number of the wiring line 22 in the 2mm field which added the array of wiring line 22a in I/O cel CELL-A of the adjoining periphery section to this, and met it at the periphery section of a chip is calculated, it will become 27 and the array consistency of the wiring line 21 will be set to mm in 13.5 [/] after all. It turns out that the array consistency of a wiring line was increased from now on as compared with conventional 12 [/mm] were shown in drawing 13 .

[0025] This divides into two or more I/O cels CELL the ball electrode 31 arranged for a chip 3, and the wiring pad 21 arranged to the package substrate 2. By arranging some of the I/O cels in the location corresponding to the periphery section of a chip 3, and

arranging other I/O cels in the location corresponding to the inner circumference section of a chip 3 When the dimension of a chip 3 is reduced and a chip is miniaturized, but the number of the ball electrode 31 and the wiring pads 21 is also set, when [with the same chip dimension] it increases. On the top face of the package substrate 2, the drawer of the wiring line 22 to the circumference outside field of a chip 3 becomes possible, and the semiconductor device corresponding to high integration of a semiconductor device and high-performance-izing can be realized. As especially shown in drawing 3 , since it does not pass through the wiring line of other I/O cels, I/O cel CELL-B arranged in the inner circumference section of a chip can be arranged in the shape of endless (annular) in the inner circumference section of a chip, and the array of many ball electrodes 31 and the wiring pad 21 is attained extremely. Of course, it is possible to prepare proper spacing also between I/O cel CELL-B of the inner circumference section. Moreover, the array of the ball electrode 31 and the wiring pad 21 is attained within limits which secure the spacing SPACE at which it passes through the wiring line 22 of I/O cel CELL-B of the inner circumference section, and I/O cel CELL-A of the periphery section can cope with high integration of the above mentioned semiconductor device, and high performance-ization. Therefore, as long as the requirements for an array which was described above are satisfied, it becomes possible to arrange the I/O cel CELL freely in the field of a chip 3, and the degree of freedom in a chip design and a package design becomes large.

[0026] Moreover, with this operation gestalt, since said wiring pad 21 and the wiring line 22 are formed by the electric conduction film of one layer formed in the top face of said package substrate 2, it becomes possible for the wiring line especially connected to the same I/O cel not to cross up and down, and to perform impedance matching in each wiring line easily. When two or more wiring pads and wiring lines corresponding to close and an output buffer are especially intermingled in one I/O cel, the mutual intervention between the wiring lines of each close and output buffer is prevented, and proper impedance matching becomes possible.

[0027] Drawing 4 is the whole semiconductor device sectional view and the enlarged drawing of an important section of the 2nd operation gestalt of this invention. In addition, the same sign is given to the part equivalent to the 1st operation gestalt. With this operation gestalt, although it is the same as the 1st operation gestalt for a semiconductor device 1 to be equipped with package substrate 2A and the chip 3 carried on said package substrate 2A, and to be constituted, said package substrate 2A is the configuration whose central core layer 211 was pinched in the up-and-down build up layer 212,213, and many wiring pads 21 are formed in that top face with the electric conduction film. Moreover, said wiring pad 21 is connected even to the lower layer build up layer 213 through the through hole 23 which was connected to the wiring line of each multilayer wiring layer of the upper build up layer 212, and was established in said core layer 211. Furthermore, it connects with the ball electrode 24 for mounting formed in the underside of said lower layer build up layer 213, i.e., the underside of said package substrate 2A.

[0028] Among each build up layer of said upper and lower sides, especially the upper build up layer 212 consists of wiring layers of five layers here, said wiring pad 21 and GND layer 1G are formed by 201, GND layer 3G and VDD layer 3V are formed by the 3rd layer, and GND layer 5G connected to the through hole of said core by the 5th layer and VDD layer 5V are formed. [layer / 1st] Moreover, the 2nd layer and the 4th layer are constituted as independent wiring lines 22a and 22b for signals, respectively. Namely, with this 2nd operation gestalt, each wiring line currently formed in one layer in said 1st operation gestalt is divided and formed in each wiring layers 201-205 of the

1-5th layer. The wiring line especially connected to the wiring pad 21 as a switch terminal (signal terminal) has composition pulled out in the condition of having dissociated as each wiring lines 22a and 22b of the 2nd layer and the 4th layer.

[0029] the I/O cel CELL constituted from arrangement (it cannot be overemphasized that the same is said of the ball electrode 31 of a chip 3) of the wiring pad 21 as a group in response to multilayering (two-layer-izing) of such wiring lines 22a and 22b as typically shown in drawing 5 -- further -- the 1st -- I/O cel CELL-1 and the 2nd -- it divides into I/O cel CELL-2. and the 1st -- while arranging a part of I/O cel CELL-1A of I/O cel CELL-1 to the field corresponding to the periphery section of a chip 3, other I/O cel CELL-1B of 1st I/O cel CELL-A is arranged to the inside. And spacing for letting the wiring line 22 pulled out from I/O cel CELL-1B of said inside among 1st I/O cel CELL-1A left behind outside pass is secured. the 1st here arranged corresponding to the periphery section of a chip -- it is considering as the configuration which has arranged I/O cel CELL-1 to an outside and the inside by turns alternately [of a hoop direction], and has arranged said I/O cel CELL-1A and CELL-1B. moreover, the 2nd -- I/O cel CELL-2 -- said 1st [the], while arranging to the field corresponding to the inner circumference section of a chip rather than I/O cel CELL-1 the 2nd concerned -- some cel CELL-2Bs of I/O cel CELL-2 are arranged inside other cel CELL-2A, and spacing for letting the wiring line pulled out from 2nd I/O cel CELL-2B of said inside among 2nd I/O cel CELL-2A of the outside of a parenthesis pass is secured. here -- the 2nd -- I/O cel CELL-2 -- also setting -- the 1st -- the 2nd arranged along the hoop direction of a chip like I/O cel CELL-1 -- I/O cel CELL-2 are alternately arranged to an outside and the inside by turns.

[0030] if drawing 4 is moreover referred to again -- the 1st -- it connects with the wiring layer 202 of the 2nd layer of the upper build up layer 212 in that outside field, and the wiring line 22-1 connected to the wiring pad 21-1 of I/O cel CELL-1 is pulled out by this wiring layer 202 of the 2nd layer to the external field. moreover, the 2nd -- the wiring line 22-2 connected to the wiring pad 21-2 of I/O cel CELL-1 -- that outside and the 1st -- it connects with the wiring layer 204 of the 4th layer of the build up layer 212 of said upper layer in the field between I/O cel CELL-1, and is pulled out by this wiring layer 204 of the 4th layer to the external field. therefore, the 2nd -- the wiring line 22-2 connected to I/O cel CELL-2 -- the 1st -- as [pull / through between I/O cel CELL-1 / by the external field] In addition, it cannot be overemphasized that each wiring layer 202,204 of the 2nd layer and the 4th layer is connected to the through hole 23 of a core layer 211 in a position, and it connects with the ball electrode 24 for mounting of the underside of package substrate 2A through the lower layer build up layer 213.

[0031] Thus, after dividing an I/O cel into the 1st and the 2nd I/O cel CELL-1, and CELL-2 By having arranged, respectively to the field corresponding to the periphery section and the inner circumference section of a chip 3, having divided each I/O cel into the inside and an outside, respectively, and having arranged it further Especially the wiring pad 21 in the top face of package substrate 2A, and the configuration of the wiring line 22 the 1st -- I/O cel CELL-1 and the 2nd -- the configuration same with I/O cel CELL-2 having been alike, respectively, having set, and having been shown in drawing 3 -- becoming -- the 1st -- I/O cel CELL-1 and the 2nd -- it becomes possible to improve the array consistency of each wiring pad 21 of I/O cel CELL-2, and the wiring line 22. and -- this 2nd operation gestalt -- a chip -- receiving -- the 1st -- I/O cel CELL-1 and the 2nd -- since it considers as the condition of having arranged I/O cel CELL-2 to the duplex, as compared with the array of the I/O cel of the 1st operation gestalt, a twice [about] as many array consistency as this can be obtained. When a

chip is miniaturized and a ball electrode and the number of wiring pads are increased [or] by this, the drawer of the wiring line of each I/O cel becomes possible, and the semiconductor device corresponding to high integration of a semiconductor device and high-performance-izing can be realized.

[0032] The wiring line 22-1 of I/O cel CELL-1 is pulled out by the wiring layer 202 of the 2nd layer. moreover -- this 2nd operation gestalt -- the 1st -- the 2nd -- the wiring line 22-2 of I/O cel CELL-2, since it is pulled out by the wiring layer 204 of the 4th layer It becomes possible to pull out the wiring line connected to each I/O cel in the same wiring layer, and for the wiring line of one I/O cel not to cross up and down, and to perform impedance matching in each wiring line easily. Especially the thing that the mutual intervention between the wiring lines of each close and output buffer is prevented, and proper impedance matching becomes possible when two or more wiring pads and wiring lines corresponding to close and an output buffer are intermingled in one I/O cel is the same as that of the 1st operation gestalt.

[0033] in addition, the 1st in this 2nd operation gestalt -- I/O cel CELL-1 and the 2nd -- what is shown in drawing 6 can be considered as an arrangement gestalt of I/O cel CELL-2. (a) of this drawing -- the 1st -- it arranges only about I/O cel CELL-1 as outside I/O cel CELL-1A and inside I/O cel CELL-1B. moreover, this drawing (b) -- the 2nd -- it arranges as an I/O cel CELL-2B of outside I/O cel CELL-2A and the inside only about I/O cel CELL-2. of course, this drawing (c) -- like -- the 1st -- I/O cel CELL-1 and the 2nd -- it is also possible to arrange I/O cel CELL-2 by the single tier, respectively. Moreover, as shown in drawing 7 , either the 1st I/O cel or the 2nd I/O cel is not constituted as an I/O cel, but it is good also as a conventional peripheral condition. this drawing (a) -- the periphery section -- peripheral one PL -- constituting -- the inner circumference section -- the 2nd -- as I/O cel CELL-2 -- constituting -- this drawing (b) -- further -- the 2nd of the inner circumference section -- I/O cel CELL-2 are arranged as an I/O cel CELL-2B of outside I/O cel CELL-2A and the inside. moreover, this drawing (c) -- the periphery section -- the 1st -- although constituted as I/O cel CELL-1, the inner circumference section consists of peripheral one PL. in this case, this drawing (d) -- like -- the 1st -- I/O cel CELL-1 may be arranged as outside I/O cel CELL-1A and inside I/O cel CELL-1B.

[0034] moreover, as the arrangement corresponding to drawing 7 (a) - (d) is shown in drawing 8 (a) - (d), there is 1st I/O cel CELL-1 -- showy [be and] -- the 2nd -- it is good also as a configuration which constituted a part of I/O cel CELL-2 from peripheral one PL, and was intermingled in the I/O cel CELL and peripheral one PL. **** 1 I/O cel CELL-1 (CELL-1A, CELL-1B) which similarly consists of an inside I/O cel and an outside I/O cel as shown in drawing 9 (a) - (d), or the 2nd -- a part of I/O cel CELL-2 (CELL-2A, CELL-2B) may consist of peripheral ones PL. As compared with a configuration, buildup of a ball electrode and the number of wiring pads is conventionally [which was shown in drawing 12] possible, and, in any case, high integration of a semiconductor device and high performance-ization can be realized.

[0035] Also in which semiconductor device of the 1st of a more than, and the 2nd operation gestalt, although the approach for arranging as an I/O cel is the same as the ball electrode 31 and the wiring pad 21 were described above, here explains the configuration method of the semiconductor device of the 1st operation gestalt with reference to the flow chart of drawing 10 especially. First, the template which put in order the I/O cel which it is going to arrange in a chip, and peripheral one along with the periphery section of a chip is created (S101). Next, in this template, it judges whether an I/O cel, a peripheral ball electrode and the number of wiring pads, and the number of terminals demanded are reached (S102). When having reached the number

of terminals demanded, it judges whether the center section of the chip also has the demand which arranges an I/O cel (S103), and arrangement is ended when there is no demand (S104). When a chip center section also has the demand which arranges an I/O cel, a cel is moved so that a floor plan may be met (S105), and in being movable, it ends arrangement (S104). when it cannot move, after changing a floor plan and an I/O cel -- (S106) -- step S105 is performed again. It shifts to step S108 which mentions this processing later as a multiple-times line when it cannot move.

[0036] When having not reached the number of terminals to demand in said step S102, in order to make it increase to the number of which the number of terminals is required on the other hand, the number of the I/O cels arranged in the inner circumference section of a chip is computed (S107). Moreover, the template which shortened between I/O cels continuously is newly created (S108). And an I/O cel is moved so that a floor plan may be met (S109). If all I/O cels are movable at this time, as described above, it will be possible to arrange an I/O cel in the periphery section and the inner circumference section of a chip, respectively, and arrangement will be ended (S104). When at least one is [of an I/O cel] unmovable, after creating the template which shortened between I/O cels further, (S110) and step S109 are performed again. Or after changing a floor plan and an I/O cel if needed, step S109 is performed again. And after making this rerun impossible [arrangement] when I/O cels are moved [no] and arrangement is completed as a multiple-times line, and expanding the chip size or increasing the number of wiring layers, it redoes from the first step S101 (S110).

[0037] In addition, in the case of the 2nd operation gestalt, to insert the processing which divides an I/O cel into the 1st I/O cel and the 2nd I/O cel, and what is necessary is made just to perform processing after step S108 among said steps S107 and S108 about each I/O cel, respectively.

[0038] In such a configuration method, a switch terminal, V terminal, and G terminal are made into the group of a bundle, and this is made into an I/O cel, and when the propriety of the drawer of a wiring line can be easily judged to the creation time of a floor plan and TAT is shortened by determining uniquely how pulling out the wiring line connected to the array of the wiring pad about this I/O cel, and each wiring pad etc., it becomes advantageous. Moreover, it is also possible by using I/O of a different application properly, after making the application of each I/O cel etc. hold as information to customize easily for every class of semiconductor device.

[0039] Here, although said each operation gestalt showed the example of 4x3 as an example of arrangement of an I/O cel, it is possible to constitute as an I/O cel of the matrix configuration of the number of arbitration. Moreover, it cannot be overemphasized that it is possible to arrange two or more conventional peripheral one depending on the case, and to constitute as an I/O cel.

[0040] Moreover, although the example which applied this invention to each arrangement of the ball electrode 31 formed in the underside of a chip 3, the wiring pad 21 formed in the package substrates 2 and 2A, and the wiring line 22 was shown with said each operation gestalt when drawing 1 and drawing 4 were referred to It is possible to apply this invention similarly about the ball electrode 24 for mounting of a semiconductor device 1, and the wiring pad 41 and wiring line of the substrate 4 for mounting. that is, while increase the array consistency of the ball electrode 24 for these mounting, and a wiring pad 41 and attaining the miniaturization of the package of a semiconductor device 1 by arranging the wiring pad 41 of the top face of the package substrate 2 of a semiconductor device 1, and the ball electrode 24 for mounting formed in the underside obtained two and the substrate 4 for mounting as an I/O cel, respectively, it becomes possible to increase the number of terminals, and high

integration of a semiconductor device and advanced features can be realized. In addition, in this case, when applying the 2nd operation gestalt, the substrate 4 for mounting will be constituted as multilayer-interconnection structure.

[0041]

[Effect of the Invention] While this invention divides electrode terminals, such as a ball electrode, into an I/O cel as explained above, and arranging some of the I/O cels in the location by the side of the periphery section of carried members, such as a chip [since other I/O cels were arranged in the location by the side of the inner circumference section rather than it, when a chip is miniaturized] Or when the number of ball electrodes is increased, the drawer of the wiring line from the wiring pad corresponding to each I/O cel to the circumference outside of a chip becomes possible, and the semiconductor device corresponding to high integration of a semiconductor device and high-performance-izing can be realized.

[0042] Moreover, since the wiring pad and wiring line corresponding to an I/O cel in this invention are formed by the electric conduction film of one layer formed in the substrate, it becomes possible for the wiring line especially connected to the same I/O cel not to cross up and down, and to perform impedance matching in each wiring line easily. Moreover, since the I/O cel was divided as the 1st I/O cel and the 2nd I/O cel, these I/O cels are arranged to the periphery section [of a chip], and inner circumference section side and each I/O cel is further arranged on the inside and the outside of a chip, high integration of the further semiconductor device and high performance-ization are realizable. Moreover, since it consists of wiring layers from which each wiring line corresponding to the 1st I/O cel and the 2nd I/O cel differs, even when both the I/O cel has been arranged to the periphery section [of a chip], and inner circumference section side, respectively, it becomes possible to arrange each I/O cel in an inside location and an outside location, respectively, and impedance matching in the wiring line corresponding to each I/O cel also becomes easy.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the whole semiconductor device sectional view and the enlarged drawing of an important section of the 1st operation gestalt of this invention.

[Drawing 2] It is drawing showing the array condition of the wiring pad of the top face of the package substrate of the 1st operation gestalt, and a wiring line.

[Drawing 3] It is drawing for explaining the array consistency in the wiring pad and wiring line of drawing 2 .

[Drawing 4] It is the whole semiconductor device sectional view and the enlarged drawing of an important section of the 2nd operation gestalt of this invention.

[Drawing 5] It is drawing showing the array condition of the wiring pad of the top face of the package substrate of the 2nd operation gestalt, and a wiring line.

[Drawing 6] It is the 1 of drawing showing the modification of the ball electrode of the 2nd operation gestalt, and the example of an array of a wiring pad.

[Drawing 7] It is the 2 of drawing showing the modification of the ball electrode of the 2nd operation gestalt, and the example of an array of a wiring pad.

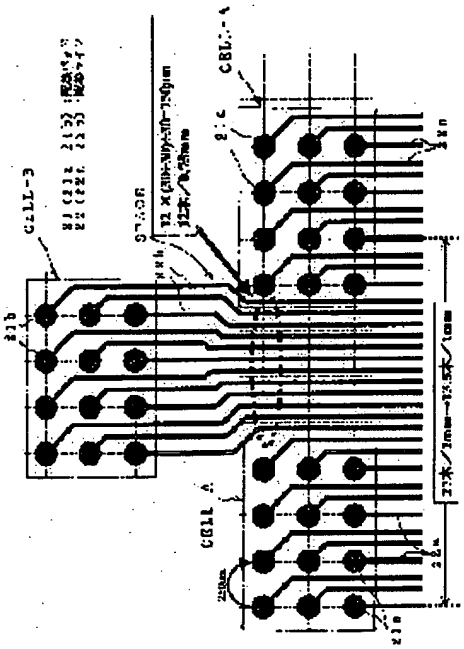
[Drawing 8] It is the 3 of drawing showing the modification of the ball electrode of the 2nd operation gestalt, and the example of an array of a wiring pad.

[Drawing 9] It is the 4 of drawing showing the modification of the ball electrode of the 2nd operation gestalt, and the example of an array of a wiring pad.

[Drawing 10] It is the flow chart which shows the manufacture approach of the semiconductor device of this invention in order of a process.
[Drawing 11] It is the sectional view of the conventional semiconductor device.
[Drawing 12] It is drawing showing the array condition of the wiring pad of the package substrate of the conventional semiconductor device, and a wiring line.
[Drawing 13] It is drawing for explaining the conventional wiring pad and the array consistency of a wiring line.
[Description of Notations]
1 Semiconductor Device
2 2A Package substrate
3 Chip
4 Substrate for Mounting
21 Wiring Pad
22 Wiring Line
23 Through Hole
24 Ball Electrode for Mounting
31 Ball Electrode
41 Wiring Pad
CELL I/O cel
CELL-A Outside (periphery section) I/O cel
CELL-B Inside (inner circumference section) I/O cel
CELL-1 1st I/O cel
CELL-1A Outside I/O cel
CELL-1B Inside I/O cel
CELL-2 2nd I/O cel
CELL-2A Outside I/O cel
CELL-2B Inside I/O cel
PL Peripheral

PATENT ABSTRACTS OF JAPAN

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD



(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device and its manufacturing method for increasing the number of terminals of a ball electrode, while miniaturizing a chip or the like in a semiconductor device, in a configuration where the ball electrode provided at the chip or the like is connected to a wiring pad provided at a package substrate or the like.

SOLUTION: In this semiconductor device where a plurality of ball electrodes are arranged and formed into a chip, and a wiring pad 21 where the ball electrodes are connected is formed at a package substrate for mounting the chip, a plurality of I/O cells CELL, where the wiring ad 21 corresponding to the plurality of ball electrodes including at least the ball electrode for signal lines are composed, the I/O cells are set to CELL-A and CELL-B, and are arranged at a position on the side of the outer-periphery part of the chip and at a position on the side of the inner-periphery part. Even when the scale of the chip is increased or even when the number of ball electrodes is increased, a wiring line can be withdrawn from a wiring pad corresponding to each I/O cell to the outside of the periphery of the chip, thus realizing a semiconductor device corresponding to high integration and to high performance of the semiconductor device.